Anurag Kar

+1(404)645-4463 | anurag.kar@gatech.edu | linkedin.com/in/anuragkar09 | anuragkar09.github.io | Google Scholar

Education

Ph.D. in Computer Science 2022 – 2027 (expected)
Georgia Institute of Technology | GPA – 4.0/4.0 *Atlanta, GA*
Advisor: Professor Hyesoon Kim

M.S. in Computer Science 2021 – 2023 (expected)
Georgia Institute of Technology | GPA – 4.0/4.0 *Atlanta, GA*

B.Tech and M.Tech in Electronics and Communication Engineering 2013 – 2018
Indian Institute of Technology - Kharagpur | GPA – 8.8/10 *West Bengal, India*

Research Experience

HPArch Lab - Georgia Institute of Technology Aug 2021 – Present
Graduate Research Assistant (advisor: Prof. Hyesoon Kim) *Atlanta, GA*

- Secure NoC Design for Side-Channel Resilience:
  - Proposed an encryption and remapping based mitigation technique for NoC side-channel resilience.
  - Achieved 94% reduction in variance with only 7% performance overhead.
  - Paper published in IEEE Computer Architecture Letters
- Memory Safety:
  - Did security analysis for a novel memory safety mechanism which utilizes Static Taint Analysis. Ran Juliet Test Suite for C/C++ and ran tests on gem5 simulator. Wrote up the results for a paper draft.
  - Working on RISC-V implementation of the QARMA block cipher using Chisel for the implementation part of the paper. Paper is planned to be submitted to USENIX Security in Feb 2022
- Mitigating Power Side Channel Attacks Using DVFS:
  - Modified Macsim architectural simulator to support dynamic frequency scaling and fixed existing bugs
  - Working on power modelling of Intel GPU by correlating power measurements with simulation statistics

Australian National University May 2017 – Jul 2017
Research Intern (advisors: Prof. H.H. Tan and Prof. Chennupati Jagadish) *Canberra, Australia*

- Worked with Prof. Chennupati Jagadish and Dr. Dipankar Chugh to investigate single photon emitters from NV centres in hexagonal Boron Nitride
- Characterized samples using Photoluminiscence, Raman and g2 measurements. Analysed data using MATLAB.

VLSI Engineering Lab - IIT Kharagpur Jul 2016 – May 2018
Student Researcher (advisor: Prof. Prasanta Kumar Guha) *Kharagpur, India*

- Worked with Prof. P.K. Guha and Dr. Sayan Dey to create a Cr(VI) sensor with a limit of detection of 125 ppb
- Presented the results in an oral presentation at the EMRS Spring Meet 2017 in Strasbourg, France
- Published a paper based on this work in IEEE Transactions on Electron Devices journal

Industry Experience

Research Intern May 2023 – Aug 2023
AMD *Austin, USA (Internship)*

- Worked on novel PIM architectures for next gen AMD SoCs, specifically related to coherence issues in PIM

Engineering Intern - CPU Modelling May 2022 – Aug 2022
Qualcomm *Santa Clara, USA (Internship)*

- Worked on Qualcomm's internal CPU functional modelling tool to enable Arm SVE instructions
- Debugged and fixed existing issues with the disassembler and instruction decoder

CPU Verfication Engineer Dec 2019 – Aug 2021
ARM *Bengaluru, India (Full-time)*

- Ran RIS (Random Instruction Sequence) tools on emulator and FPGA and caught system level bugs
- Filed a bug which was categorized High Severity and resulted in erratum being added to the end user manual
- Wrote programs in Perl and Python to automate regression and debug tasks and also contributed to the repositories for all the internal tools used

- Wrote stimulus in C and ARM Assembly language to test specific blocks of the microarchitecture

System Validation Engineer Jul 2018 – Dec 2019

Intel Corporation *Bengaluru, India (Full-time)*

- Developed a python library of portable functions for test automation and debug. Library is widely in use by Intel teams across the globe in India, Israel and the U.S.
- Received a formal recognition for contribution to the latest Intel SoC bring up in Hillsboro, Oregon
- Part of the SoC debug task force, involved in working with several teams across Intel globally to work on critical debug issues and to come up with fixes

Publications

- Y. Kim, **A. Kar**, J. Lee, J. Lee, and H. Kim, "RV-CURE: A RISC-V Capability Architecture for Full Memory Safety," arXiv preprint arXiv:2308.02945, 2023.
- Y. Kim, **A. Kar**, J. Lee, J. Lee and H. Kim, "Hardware-Assisted Code-Pointer Tagging for Forward-Edge Control-Flow Integrity," in IEEE Computer Architecture Letters, vol. 22, no. 2, pp. 117-120, July-Dec. 2023, doi: 10.1109/LCA.2023.3306326
- **A. Kar**, X. Liu, Y. Kim, G. Saileshwar, H. Kim and T. Krishna, "Mitigating Timing-Based NoC Side-Channel Attacks With LLC Remapping," in IEEE Computer Architecture Letters, vol. 22, no. 1, pp. 53-56, Jan.-June 2023, doi: 10.1109/LCA.2023.327670
- Yonghae Kim, **Anurag Kar**, Siddhant Singh, Ammar A. Ratnani, Jaekyu Lee and Hyesoon Kim, "AOS-RISC-V: Towards Always-On Heap Memory Safety," in Workshop on Computer Architecture Research with RISC-V (CARRV 2022) Jun. 2022
- **A. Kar**, S. Dey, D. Burman, S. Santra and P. K. Guha, "RGO/Ni2O3 Heterojunction-Based Reusable, Flexible Device for Cr(VI) Ion Detection in Water," in IEEE Transactions on Electron Devices, vol. 68, no. 2, pp. 780-785, Feb. 2021, doi: 10.1109/TED.2020.3045954

Talks and Presentations

- "NOICER: Mitigating NoC Side-Channel Attacks with address encryption and remapping", IEEE/ACM International Symposium on Networks-on-Chip (NOCS) Oct. 2022.

Academic and Professional Achievements

2022	DAC Young Fellow, IEEE Design Automation Conference (travel grant + fee waiver worth $1000)
2021	'Bravo' award for automating debug critical System Verilog Assertion flow for CPU verification on FPGA
2019	Recognized by the Intel Thunderbolt team in Oregon for contribution to SoC power-on activities
2017	Chennupati and Vidya Jagadish Endowment for research at Australian National University
2014	National Initiative for Undergraduate Sciences (NIUS) Physics scholar, India
2013	Among 12 students from state of Gujarat, India selected for the Indian National Physics Olympiad
2009	Duke University Talent Identification Program (Duke TIP) scholar for academically gifted high-school students

Skills and Relevant Courses

Relevant Courses: High Performance Computer Architecture, Reliable and Secure Computer Architecture, Advanced Operating Systems, Interconnection Networks, Quantum Computing, Graduate Algorithms
Subject Knowledge: Computer Architecture, Arm ISA, Operating Systems, Memory Security, Architectural Security, Digital Design, CPU Verification, Post Silicon Debug, Electronic Materials Characterization
Languages: C/C++, Python, Perl, Scala, Matlab, Verilog

Academic Service and Teaching

- Submission Chair for International Symposium on Computer Architecture, 2023 (ISCA)
- Artifact Evaluation Committee Member for IEEE International Symposium on High-Performance Computer Architecture, 2022 (HPCA)
- Graduate Teaching Assistant for Processor Design (CS3220) at Georgia Tech for Spring '22 and Spring '23 semesters